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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,955	08/17/2005	Craig J. Boucher	EBA-0022	2081

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EXAMINER	
KITOV, ZEEV V	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,955	BOUCHER, CRAIG J.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/09/06, 01/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1- 5, 7, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baginski (US 6,192,802) in view of Parat et al. (US 5,877,927). Regarding Claim 1, Baginski discloses an initiator (Fig. 1 Fig. 6) having input nodes (66 and 66' in Fig. 6). It further discloses ESD protection elements (Fig. 2(A), 2(B), 2(C)) and clamping elements (Fig. 11A, 12A) connected across the input nodes (Fig. 11A, 12A). However, it does not disclose the clamping portion being controlled by the timing portion of the ESD protection circuit. Parat et al. discloses the ESD protection circuit (Fig. 2) having a clamping portion (120 in Fig. 2) letting a normal input signal to pass without clamping; and a timer (130 in Fig. 2) connected to the clamping portion and to the input nodes (100 and ground in Fig. 2) and being responsive to the input signals and issuing a release signal to the clamping portion after passage of a clamping interval determined by the timer circuit (130 in Fig. 2) after the receipt of the input signal in the input pad (100 in Fig. 2). The second reference is pertinent to the case since it discloses realization of an alternative solution for the ESD clamping device/circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to

have modified the Baginski solution by replacing the zener diodes by the transistor ESD protection clamping circuit according to teachings of Parat et al., because of following advantages of such solution: adjustable time delay, adjustable activation threshold of the clamping device and ability to clamp relatively small overvoltage values. Additionally, since the MOV in overvoltage conditions does not reduce its resistance to fraction of ohm as FET the clamping properties of the FET are substantially better than zener diodes.

Regarding Claims 2 – 4, Parat et al disclose the timing interval being selected equal to 2 microseconds (col. 5, lines 22 – 34). Duration of timing interval should be selected such to activate the clamp in a case of real ESD event and to ignore some spurious not dangerous voltage deviations. Therefore, the time delay duration presents a result effective variable, which may be optimized by experimenting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baginski solution by setting the time delay to some specific value, because as Court Decision *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) states: "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

Regarding Claim 5, Parat et al. disclose a unipolar clamping circuit (120 in Fig. 2) and unipolar timer circuit (130 in Fig. 2). According to The Authoritative Dictionary of IEEE Standard Terms, the unipolar transistor is "a transistor that utilizes charge carriers of only one polarity". Therefore, the MOSFET is a proper unipolar transistor.

Regarding Claim 7, Parat et al. disclose the ESD protection circuit used for protection of integrated circuits and therefore being a part of the integrated circuit. As to packaging a whole circuit including both the initiator and the ESD protection circuit together into a single IC, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baginski solution by manufacturing it together with the ESD protection circuit in a single package (IC), because as Court Decision *In re Larson,* 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) states: "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice."

As per Claim 8, it differs from Claims 1 and 7 rejected above by its limitation of some structural details of mounting the initiation element and the protective element. Baginski discloses an electro-explosive device protected against ESD having the initiative element and protective circuit being mounted on a header (62 in Fig. 6) with two electrical leads (66 and 66' in Fig. 6) connected to the protective circuit (Fig. 11A and 12A) and further including a shell (68 in Fig. 6) mounted an the header and a charge of reactive material (69 in Fig. 6) in the shell.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baginski in view of Parat et al. and Avery et al. (US 6,501,632). Claim 6 differs from Claim 1 rejected above by its limitation of using bipolar transistors. Avery et al. disclose the ESD protection circuit having the clamp portion formed by NMOS transistor with parasitic NPN transistor (in Fig. 3) and the timer portion formed by zener diodes (Z1, Z2 in Fig.

34) and parasitic zener diode resistance (Rz1 in Fig. 3). Both the clamp and the timer circuits are based on bipolar junction technology. The reference has the same problem solving area, namely providing ESD protection for the semiconductor circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Baginski solution by replacing the MOSFET elements by their bipolar junction equivalents according to teachings of Avery et al., because such solution has a number of advantages, such as: (I) the MOSFET/NPN clamp has an advantage of being extremely sensitive as MOSFET to the gate voltage (practically no current is necessary) and at the same time being able to withstand higher values of voltages and currents than MOSFET; (II) the zener diodes biasing and timing circuit according to Avery et al. (col. 3, lines 20 – 35), has an advantage of enabling the nMOS transistor to be biased to optimum conditions for bipolar snapback.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
2/16/2007

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